

FIG. 1

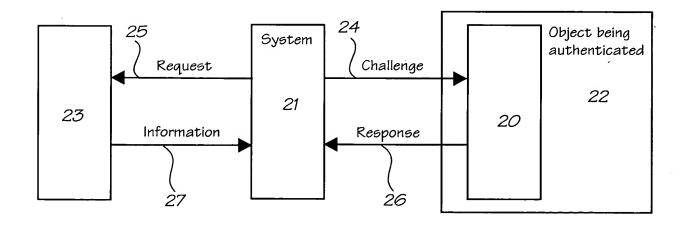


FIG. 2

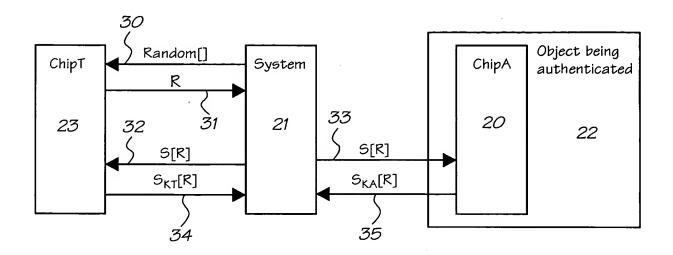


FIG. 3

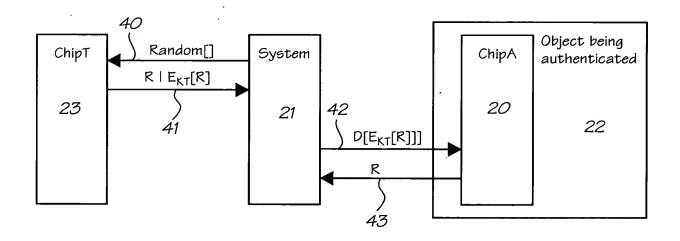


FIG. 4

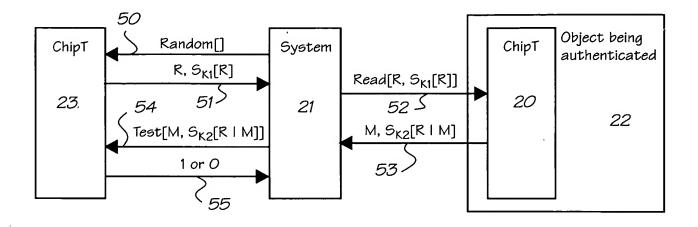


FIG. 5

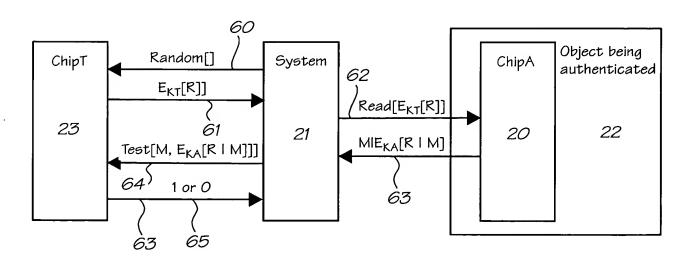


FIG. 6

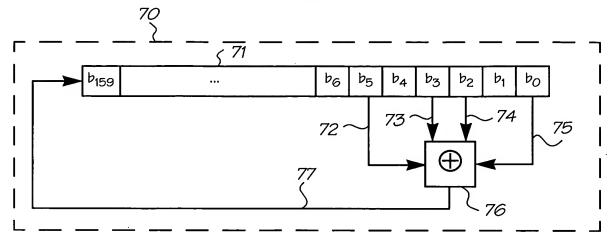
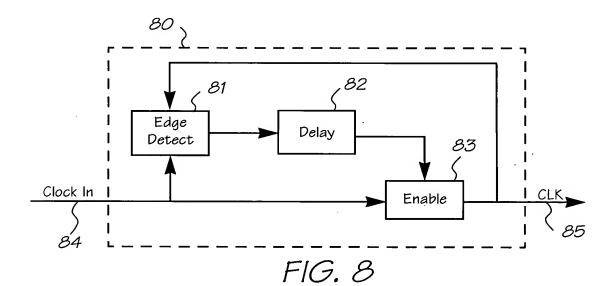
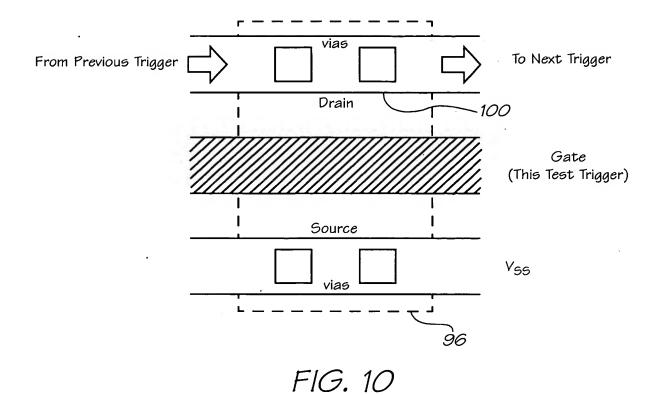


FIG. 7



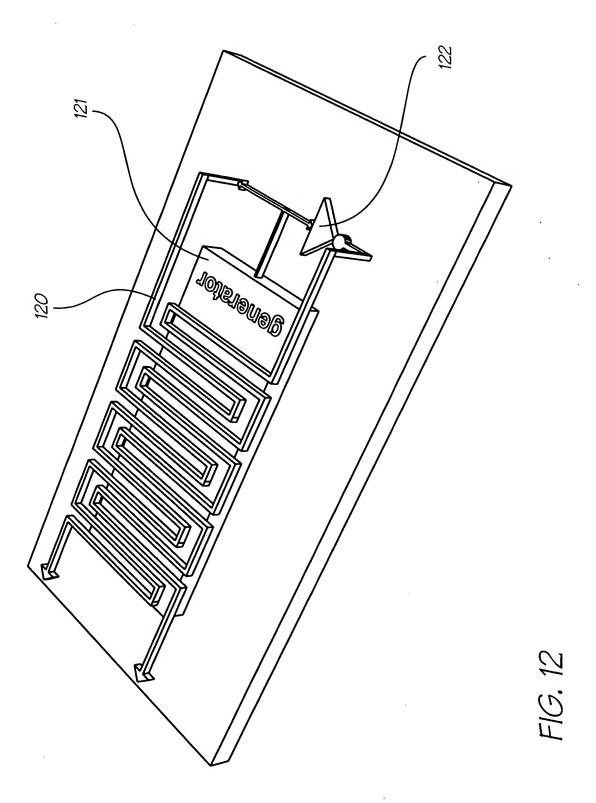
90 Random Bit Source TO ERASE Testn TestA TestB or RESET 95 94 93 Testc Test Testn 96

FIG. 9



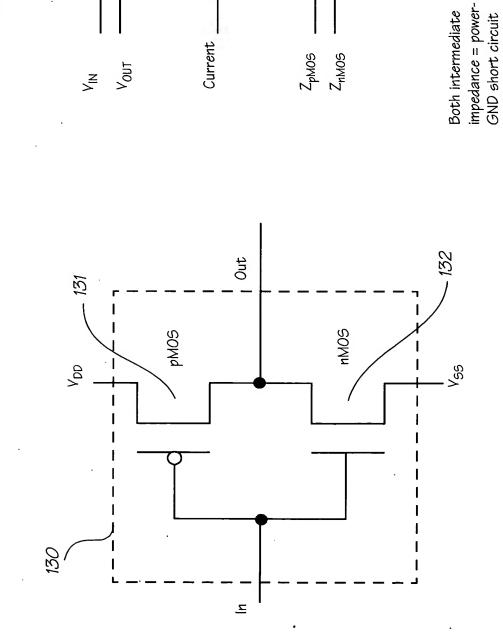
♠ ChipOK₁ $ChipOK_2$ 110 . 110 96 96 90 Random etc Bit Test Test Source 96 96 Test Test 110 110 ChipOK₃ ChipOK₄

FIG. 11



End of transition

Start of transition



Current

Vour

×Z

Z_{PMOS} Z_{nMOS}

24

